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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,836	06/27/2003	Naoto Akiyama	029437-0102	4820

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EXAMINER	
HU, SHOUXIANG	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 05/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/606,836	AKIYAMA, NAOTO	
	Examiner	Art Unit	
	Shouxiang Hu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *11-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 June 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 11-18 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 20040311.

Accordingly, claims 1-18 are pending in this application; and claims 1-10 remain active in this Office action.

Drawings

2. Figure 18 is objected to as it should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claims 1-10 are objected to because of the following informalities and/or defects:

Claim 1 recites the subject matter that the recited transistors are to be operated by a voltage generated by a same power source, but fails to clarify whether the voltage is same for all of the transistors, and to which terminal of the recited transistors the recited voltage is applied on.

Claim 1 recites the subject matter that one of the recited transistors serves as the recited power source protection element: however, according to the specification and the drawings (see the Mpcore portion in Fig. 2), the one serves as the power source protection element is actually a MOS diode.

Claim 1 recites that "said plurality of transistors including transistors thickness of which is different from each other", but fails to definitely define whether the transistors or the thickness are/is meant to be different from each other.

In claim 1, the term of "transistors thickness" seemly should be read as: --transistor thickness--.

In claims 1, 2, 7, and 9, the term "of which" should read as: --which--.

Claims 2, 7 and 9 each recites the subject matter that two of the gate dielectric layers recited in claim 1 can have a same thickness, which seems to contradict to what is defined in claim 1 which seemly requires that they are different from each other.

In claims 5 and 10, the term of "I/O port" should read as: --I/O port area--

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1-10 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter

which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 1 recites the subject matters that "said plurality of transistors including transistors thickness of which is different from each other", but the disclosure lacks an adequate description regarding how the thickness of each of the recited transistors is defined, given the fact that transistors in an IC chip normally have a common planarized passivation layer and/or multiple interconnection layers covering their gate electrodes.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claim 1, insofar as being in compliance with 35 U.S.C. 112 and as being best understood in view of the claim objections above, is rejected under 35 U.S.C. 102(e) as being anticipated by Lin et al. ("Lin"; US 2003/0173630).

Lin discloses a semiconductor device (see Fig. 5; also see Paragraphs 0041-0045), comprising: a substrate (30); and a plurality of transistors formed on the substrate to be operated by a voltage generated by a same power source, each of said

transistors having a different gate dielectric layer thickness, wherein one of the plurality of transistors that has the thinnest gate dielectric layer (under gate 20a) serves as a power source protection element.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 5, insofar as being in compliance with 35 U.S.C. 112 and as being best understood in view of the claim objections above, is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin.

The disclosure of Lin is discussed as applied to claim 1 above.

Although Lin does not expressly disclose that the transistors can be surrounded by an I/O port area, one of ordinary skill in the art would readily recognize that an IC chip commonly comprises such an I/O port area to provide required input/output functions, as evidenced in the prior art such as Nojiri (US 2001/0045670; see the I/O port area 152 in Fig. 11; also see Paragraph 0010).

Therefore, it would have been obvious to one of ordinary skill in he art at the time the invention was made to incorporated an art-known I/O port area into the semiconductor device of Lin, so that a semiconductor device with required input/output functionalities would be obtained.

10. Claims 2-4 and 6-10, insofar as being in compliance with 35 U.S.C. 112 and as being best understood in view of the claim objections above, are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art ("AAPA") in view of Lin and/or Chen et al. ("Cheng"; US 6,465,308).

AAPA discloses a semiconductor device (Fig. 18; also see Pages 1-3 of the specification) comprising: a plurality of transistors (naturally formed on a substrate) to be operated by a voltage generated by a same power source, wherein the plurality of transistors include a high speed processing type transistor (Mcore), a low power consumption type transistor (Lcore), and a transistor selected to serve as the power source protection element (Mpcore).

AAPA does not disclose that the gate dielectric layer in the transistor serving as the protection element can be thinner than that of the other ones, and/or that the threshold voltage of the transistor serving as the protection element can be higher than that of the other ones. However, as evidenced in Lin (who's disclosure is discussed as applied to claims 1 and 5 above; see the thinner gate dielectric layer under gate 20a in Fig. 5; also see Paragraphs 0041-0045), the gate dielectric layer (under gate 20a) in the transistor serving as the protection element can be desirably thinner than that of the other ones for quicker triggering of the protection element. And, as evidenced in Cheng (see col. 5, lines 25-37), the threshold voltage of the protection element is an art-recognized parameter of importance subject to routine experimentation and optimization, depending on the application voltages.

Therefore, it would have been obvious to one of ordinary skill in he art at the time the invention was made to make the semiconductor device of AAPA with the protection element's gate dielectric layer being thinner than that of the other ones, and/or that the protection element's threshold voltage being higher than that of the other ones, per the teachings of Lin and/or Cheng, so that a semiconductor device with quicker triggering and/or being suitable to high voltage applications would be obtained.

Regarding claims 3 and 4, it is noted that the process limitations about the manufacturing method recited therein would not carry patentable weight in the claims drawing to a structure, because distinct structure is not necessarily produced. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985). And, it is art-known that each gate dielectric layer can be formed with multiple dielectric layers for improving the transistor performance.

Regarding claim 8, the leak current of the transistor selected to serve as the power source protection element in the above collectively taught device would be naturally smaller than that of the high speed processing type transistor as the protection element transistor would have higher threshold voltage.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References C-F are cited as being related to a MOSFET, circuit protection, and/or I/O port structure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SH
April 29, 2004

SHOUXIANG HU
PRIMARY EXAMINER